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METHOD FOR PRODUCING A SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING A THIN FILM TRANSISTOR AND A CAPACITOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for effectively forming a contact hole and a capacitor in a semiconductor integrated circuit.

2. Description of the Related Art

In a semiconductor integrated circuit, a multilayer wiring structure is used, it is necessary to form a contact hole for connecting with wirings one another and an element such as a capacitor (condenser). To obtain the multilayer wiring structure, an interlayer insulator is formed in general, so that insulation and capacitance between the wirings are decreased. In a portion required to connect with the wirings one another, a contact hole is formed in the interlayer insulator. When a capacitor is formed, the interlayer insulator itself may be used as dielectric. However, since the interlayer insulator is used to decrease insulation and capacitance between the wirings, when the interlayer insulator is used as dielectric of the capacitor, an area of the capacitor is extremely large and thus loss is great in a circuit design.

If an interlayer insulator is thin, the capacitor having a large capacitance can be formed in the same area. However, to achieve this, it is necessary to remove the interlayer insulator completely in a contact hole forming portion and to etch the interlayer insulator suitably (until a suitable thickness required to form a capacitor) in a capacitor forming portion. Thus, it is impossible to use such the capacitor actually in mass production process.

To operate a capacitor effectively, it is required that a thickness of a portion of an interlayer insulator used as dielectric is 1/5 to 1/50 thinner than an initial thickness of an interlayer insulator. If a capacitance of a capacitor

is 100 times larger than that of an intersection portion of a normal wiring and an interlayer insulator formed in a portion of the capacitor has the same thickness as the intersection portion of the normal wiring, it is required that an area of the capacitor is 1000 times larger than that of the intersection portion of the wiring. On the other hand, if a thickness of the portion of the capacitor is 1/10, the area of the capacitor is 100 times larger than that of the intersection portion, and thus it is effective in integration of elements. However, for example, it is impossible to etch an interlayer insulator by 90 % in thickness to and remain it by only 10 % in thickness. Thus, precision control cannot be performed substantially in a desired area.

SUMMARY OF THE INVENTION

In the present invention, an interlayer insulator is constructed by at least two materials (such as an upper layer and a lower layer) each having different dry etching characteristics. When the upper layer is etched by dry etching, a thickness of the lower layer can be controlled precisely by using the lower layer as an etching stopper. By using a first mask, a desired region in the upper layer can be etched selectively.

After the desired region in the upper layer is etched and removed, the lower layer is etched selectively using a second mask in a contact hole forming portion. This etching process may be dry etching or wet etching. In a capacitor forming portion, the lower layer is covered with a mask to prevent etching. In an etching condition for the lower layer, when the upper layer is not etched sufficiently, the second mask may be used to expose a portion other than the portion etched by using the first mask.

In particular, in the present invention, when the interlayer insulator has two layer structures wherein the upper layer is formed by a material containing mainly

3

silicon nitride and the lower layer is formed by a material containing mainly silicon oxide, it is superior because dry etching characteristics are different largely each other.

A transparent conductive material such as ITO (indium tin oxide) may be used as the second mask. For example, a pixel electrode in a TFT array of an active matrix type liquid crystal display can be used as the second mask. In this case, a photolithography process can be omitted.

According to the present invention, there is provided a method for producing an semiconductor integrated circuit comprising the steps of: forming an interlayer insulator including at least upper and lower layers each having different dry etching characteristics; etching the upper layer of the interlayer insulator using a first mask, wherein the lower layer of the interlayer insulator is used as an etching stopper; forming a second mask to cover a portion of the lower layer of the interlayer insulator exposed by the etching step; selectively etching the lower layer of the interlayer insulator using the second mask; forming a contact hole in one portion that the upper and lower layers of the interlayer insulator are etched; and forming a capacitor in another portion that only the upper layer of the interlayer insulator is etched.

According to the present invention, there is provided a method for producing an semiconductor integrated circuit comprising the steps of: forming an interlayer insulator including upper and lower layers, wherein the upper layer has silicon nitride and the lower layer has silicon oxide; etching the upper layer of the interlayer insulator using a first mask, wherein the lower layer of the interlayer insulator is used as an etching stopper; forming a second mask to cover a portion of the lower layer of the interlayer insulator exposed by the etching step; selectively etching the lower layer of the interlayer insulator using the second mask; forming a contact hole in one portion that the upper

and lower layers of the interlayer insulator are etched; and forming a capacitor in another portion that only the upper layer of the interlayer insulator is etched.

According to the present invention, a thickness of dielectric of a capacitor is determined by a thickness of a lower layer of an interlayer insulator. In an upper layer etching process, since the lower layer serves as an etching stopper, the thickness of dielectric of a capacitor can be uniform in an entire area. When a thickness of the lower layer of the interlayer insulator is 1/5 to 1/50 of an entire thickness of the interlayer insulator, since a thickness of dielectric of the capacitor can be sufficiently thin, it is effective to reduce an area of the capacitor. When a dielectric constant of a material used in the upper layer is different from that of a material used in the lower layer, it is necessary to consider its effect.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1E show a process for producing a thin film transistor (TFT) according to Embodiment 1;

Figs. 2A to 2E show a process for producing a TFT according to Embodiment 2;

Figs. 3A to 3E show a process for producing a TFT according to Embodiment 3;

Figs. 4A to 4F show a process for producing a TFT according to Embodiment 4; and

Figs. 5A to 5F show a process for producing a TFT according to Embodiment 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment 1

Figs. 1A to 1E show a process for producing one pixel in a thin film transistor (TFT) array of an active matrix circuit used in a liquid crystal display device, according to the embodiment.

A silicon oxide film 102 having a thickness of 1000 to 5000 Å, for example, 4000 Å, is formed as a base oxide film

on a substrate 101 such as a glass substrate (Corning 7059). After an amorphous or crystalline island silicon region having a thickness of 100 to 1500 Å, for example, 800 Å is formed, a gate insulating film 104 is formed by a silicon oxide having a thickness of 1200 Å.

A polycrystalline silicon film having good conductivity obtained by introducing phosphorus at a desired quantity is formed at a thickness of 3000 Å by low pressure chemical vapor deposition (LPCVD) and then etched to form a gate electrode 106 and lower layer wirings 105 and 107. Then, by ion doping, an impurity (phosphorus in the embodiment) is implanted into the island silicon region using the gate electrode 106 as a mask in a self-alignment, to form impurity regions 103. The impurity region may be formed before the gate electrode is formed. (Fig. 1A)

A silicon oxide film 108 having a thickness of 200 to 1000 Å, for example, 500 Å, is formed by plasma CVD, and then a silicon nitride film 109 having a thickness of 2000 to 10000 Å, for example, 5000 Å is formed by plasma CVD, thereby to form an interlayer insulator. (Fig. 1B)

Using a first mask, a pattern is formed by a known photoresist method, and then the silicon nitride film 109 corresponding to an upper layer in the interlayer insulator is etched by dry etching. By setting a suitable etching condition, the silicon nitride film 108 corresponding to the upper layer can be used as an etching stopper. Thus, hole portions 110, 111 and 112 are formed. (Fig. 1C)

Then, a hole pattern is formed again inside the hole portions 110 and 111 by photolithography using a second mask. A hole pattern is not formed in the hole portion 112. The gate insulating film 104 of a silicon oxide and the silicon oxide film 108 are etched using buffer hydrofluoric acid, to form contact holes 113 and 114. Since this etching is performed by isotropic wet etching, it is required that a size (diameter) of the contact hole 113 or 114 is smaller

than that of the hole portion 110 or 111. (Fig. 1D)

A pixel electrode 115 is formed by using an indium tin oxide (ITO) film having a thickness of 1000 Å. An aluminum film having a thickness of 5000 Å is formed by sputtering and then etched to form metal wiring-electrodes 116 and 117 corresponding to the upper layer. The metal wiring-electrodes 116 and 117 are connected to the impurity regions 103 of the TFT through the contact holes 113 and 114. In the hole portion 112, the silicon oxide film 108 corresponding to the lower layer in the interlayer insulator is used as dielectric, and a capacitor 119 is formed between the pixel electrode 115 made of the ITO film and the lower layer wiring 107. The capacitor 119 corresponds to a retaining capacitor (auxiliary capacitor) in a TFT array of an active matrix circuit.

In a portion 118 in which the upper layer wiring 116 (corresponding to a source bus line of an active matrix circuit) is formed across on the lower layer wiring 105 (corresponding to a gate bus line of the active matrix circuit), since the silicon nitride film 109 having a thickness of 5000 Å also serves as an insulator in addition to the silicon oxide film 108 having a thickness of 500 Å, sufficient insulation can be obtained. (Fig. 1E)

In the embodiment, the upper electrode of the capacitor is formed using the pixel electrode 115 made of the ITO film. It may be formed by extending the upper layer wiring 117 on the lower layer wiring 107. Also, in the embodiment, the pixel electrode 115 is formed before the upper layer metal wiring 117 is formed. It may be formed after the upper layer metal wiring 117 is formed.

Embodiment 2

Figs. 2A to 2E show a process for producing an active matrix circuit used in a liquid crystal display device, according to the embodiment.

As described in Embodiment 1, a base oxide film 202 and

an island silicon region are formed on a substrate 201 such as a glass substrate (Corning 7059), and then a gate insulating film of silicon oxide having a thickness of 1200 Å is formed. Further, an aluminum film into which scandium is mixed (added) at 0.3 weight % is formed at a thickness of 5000 Å by sputtering and then etched to form a gate electrode 206 and aluminum lower layer wirings 205 and 207. In the embodiment, as described in Japanese Patent Application Open No. 5-267667, anodization is performed in an electrolytic solution using the gate electrode 206 and the aluminum wirings 205 and 207 as anodes, so that fine anodic oxide layers having a thickness of 1000 Å are formed around the gate electrode 206 and the aluminum wiring 205 and 207. Impurity regions 203 are formed in the island silicon region in a self-alignment or a non-self-alignment. (Fig. 2A)

As described in Embodiment 1, a silicon oxide film 208 having a thickness of 300 Å and a silicon nitride film 209 having a thickness of 4700 Å are formed successively by plasma CVD. Using a first mask, hole portions 210 to 212 are formed in the silicon nitride film 209 by dry etching. In this state, the silicon nitride film 208 serves as an etching stopper, as described in Embodiment 1. (Fig. 2B)

A pixel electrode 213 is formed by an ITO film having a thickness of 500 Å. As a result, a capacitor 219 is formed wherein the pixel electrode 213 and the lower layer wiring 207 are used as both electrodes of the capacitor 219 and the anodic oxide and the silicon oxide film 208 are used as dielectric. (Fig. 2C)

Then, anisotropic dry etching by a known reactive ion etching (RIE) is performed to etch the gate insulating film 204 of silicon oxide and the silicon oxide film 208. As can be seen from Figs. 2C and 2D, a portion in which the silicon oxide film 208 is exposed is present in only the hole portions 210 and 211. since the hole portion 212 is covered

with the pixel electrode 213 made of the ITO film, it is not etched. That is, in the embodiment, the pixel electrode 213 (or a mask used to form it) serves as a second mask according to the invention. Etching has anisotropy and selectively proceeds in a direction vertical to a substrate. Thus, contact holes 214 and 215 are formed. (Fig. 2D)

An aluminum film having a thickness of 4000 Å is formed by sputtering and then etched to form upper layer wiring-electrodes 216 and 217. In a portion 218, although the upper layer wiring 216 intersects the lower layer wiring 205, since the anodic oxide having a thickness of 1000 Å is formed in addition to an interlayer insulator which is constructed by the silicon oxide film 208 having a thickness of 300 Å and the silicon nitride film 209 having a thickness of 4700 Å, sufficient insulation can be obtained. In the capacitor 219, since dielectric is thin sufficiently, it is effective to decrease a capacitor area. (Fig. 2E)

<u>Embodiment 3</u>

Figs. 3A to 3E show a process for producing one pixel in a TFT array of an active matrix circuit used in a liquid crystal display device, according to the embodiment.

A silicon oxide film 302 having a thickness of 2000 Å is formed as a base oxide film on a substrate 301. An amorphous silicon film having a thickness of 500 Å is formed, and then is irradiated with an excimer laser light, to obtain a crystalline silicon film. The crystalline silicon film is etched to form an island silicon region. A gate insulating film 304 is formed by using a silicon oxide having a thickness of 1200 Å.

A polycrystalline silicon film having good conductivity obtained by introducing phosphorus at a desired quantity is formed at a thickness of 3000 Å by low pressure CVD and then etched to form a gate electrode 306 and low layer wiring 305. Then, by ion doping, an impurity (phosphorus in the embodiment) is implanted into the island silicon region

using the gate electrode 306 as a mask in a self-alignment, to form impurity regions 303. By plasma CVD, a silicon oxide film 307 having a thickness of 2000 to 8000 Å, for example, 5000 Å, is formed as a first interlayer insulator. (Fig. 3A)

Contact holes are formed in the silicon oxide film 307 of the first interlayer insulator. An aluminum film having a thickness of 4000 Å is formed by sputtering, and then etched to form upper layer wirings 308, 309, and 310. (Fig. 3B)

By plasma CVD, a silicon oxide film 311 having a thickness of 1000 Å and a silicon nitride film 312 having a thickness of 5000 Å are formed successively as a second interlayer insulator. (Fig. 3C)

Using a first mask, a pattern is formed by a known photoresist method, and then the silicon nitride film 312 corresponding to an upper layer in the second interlayer insulator is etched by dry etching. The silicon oxide film 311 corresponding to the lower layer is used as an etching stopper. Thus, hole portions 313 and 314 are formed. (Fig. 3D)

A hole pattern is formed again inside the hole portion 313 by photolithography using a second mask. A hole pattern is not formed in the hole portion 314. By dry etching for silicon oxide, the silicon oxide film 311 in the hole portion 313 is etched to form a contact hole.

An ITO film having a thickness of 1000 Å is formed by sputtering and then etched, to form a pixel electrode 315 which is connected to the upper layer wiring 309. As described above, in the hole portion 313, the metal wiring (the drain electrode of a TFT) 309 corresponding to the upper layer is connected to the pixel electrode 315. In the hole portion 314, a capacitor 317 is formed between the ITO film 315 and the upper layer wiring 310 wherein the silicon oxide film 311 corresponding to the lower layer in the second interlayer insulator is used as dielectric. The capacitor 317 corresponds to a retaining capacitor in a TFT

array of an active matrix circuit.

In a portion 316 in which the upper layer wiring 308 (corresponding to a source bus line of an active matrix circuit) is formed across on the lower layer wiring 305 (corresponding to a gate bus line of the active matrix circuit), since the silicon oxide film (the first interlayer insulator) 307 having a thickness of 5000 Å serves as an insulator, sufficient insulation can be obtained. (Fig. 3E)

<u>Embodiment 4</u>

Figs. 4A to 4F show a process for producing an active matrix circuit used in a liquid crystal display device, according to the embodiment.

As described in Embodiment 1, a silicon oxide film 402 used as a base film and an island silicon region 403 are formed on a substrate 401, and then a silicon oxide film 404 having a thickness of 1200 Å is formed. Also, an aluminum film into which scandium is added (mixed) at 0.3 weight % is formed at a thickness of 5000 Å by sputtering. After a photoresist mask is formed, the aluminum film is etched to form a gate electrode 405 and lower layer wirings 406 and 407 of aluminum.

Without removing the photoresist mask, only the gate electrode 405 is anodized, so that a porous anodic oxide 408 having a thickness of 4000 Å is formed in the side surfaces of the gate electrode 405. Then, the photoresist mask is removed (peeled off), and the gate electrode 405 and the lower layer wirings 406 and 407 are anodized in an electrolytic solution, to form a fine anodic oxide layer 409 having a thickness of 1000 Å. (Fig. 4A)

Various anodic oxides can be formed by changing an electrolytic solution to be used. When the porous anodic oxide 408 is formed, an acid solution containing citric acid, oxalic acid, chromic acid, or sulfuric acid at 3 to 20 % is used. When the fine anodic oxide layer 409 is formed, an ethylene glycol solution containing tartaric acid, boric

acid, or nitric acid at 3 to 10 %, in which PH is adjusted to about 7 is used.

Using the gate electrode 405, the lower layer wirings 406 and 407, and the anodic oxide layers formed around them as masks, a silicon oxide film is etched to form a gate insulating film 410. After the porous anodic oxide 408 is removed, an impurity (phosphorus) is implanted into the island silicon region 403 by ion doping, using the gate electrode 405, the anodic oxide layer 409, and the gate insulating film 410 as masks. Since the gate insulating film 410 serves as a semitransparent mask, low concentration impurity regions (that is, LDDs, lightly doped drains) 411 and a high concentration impurity regions 412 are formed in the island silicon region 403 in a self-alignment. Then, by plasma CVD, a silicon oxide film 413 having a thickness of 300 Å and a silicon nitride film 414 having a thickness of 4700 Å are formed successively, to form a first insulating film. (Fig. 4B)

Using a first mask, hole portions 415, 416, and 417 are formed in the silicon nitride film 411 by dry etching. In this etching, the silicon oxide film 413 serves as an etching stopper. (Fig. 4C)

An ITO film having a thickness of 500 Å is formed and then patterned, to form a pixel electrode 418. Thus, a capacitor 419 is formed between the pixel electrode 418 and the lower layer wiring 407 wherein the anodic oxide layer 409 and the silicon oxide film 413 are used as dielectric. (Fig. 4D)

After that, by using anisotropic dry etching as known RIE, the silicon oxide film 413 is etched to from contact holes 420 and 421. As shown in Fig. 4D, portions that the silicon oxide film 413 is exposed are only the hole portions 415 and 416. Since the hole portion 417 is covered with the pixel electrode 418 made of the ITO film, it is not etched. In the embodiment, the pixel electrode 418 (or a mask used

12

to form the electrode 418 serves as a second mask. Also, since etching having anisotropy is performed selectively in a vertical direction to a substrate, contact holes 420 and 421 are formed in the hole portions 415 and 416. (Fig. 4E)

Then, an aluminum film having a thickness of 4000 Å is formed by sputtering and etched to form upper layer wiring-electrodes 422 and 423. The upper layer wiring 422 intersects the lower layer wiring 406 in a region 424. Since an interlayer insulator constructed by silicon oxide film having the thickness of 300 Å and the silicon nitride film having the thickness of 4700 Å and the anodic oxide layer 409 having the thickness of 1000 Å are formed in the region 424, sufficient insulation can be obtained. In the capacitor 419, the thickness of dielectric is sufficiently thin, and thus it is effective to reduce an area of the capacitor. (Fig. 4F)

In the embodiment, since a TFT has an LDD structure, off current characteristic can be improved. Thus, it is suitable as a TFT arranged in a pixel matrix.

Embodiment 5

Figs. 5A to 5F show a process for producing an active matrix circuit used in a liquid crystal display device, according to the embodiment. In Embodiment 4, to obtain an LDD structure, a fine anodic oxide is formed around a gate electrode. However, in the embodiment, an LDD structure is formed without forming a fine anodic oxide.

In Fig. 5A, a silicon oxide film 502 (having a thickness of 2000 Å) used as a base film and an island silicon region 503 having a thickness of 500 Å are formed on a glass substrate 501. Further, a silicon oxide film 504 having a thickness of 1000 Å is formed by plasma CVD.

An aluminum film into which scandium is added (mixed) at 0.3 weight % is formed at a thickness of 5000 Å by sputtering. The aluminum film is used to form a gate electrode 505 and a lower layer wiring 506 in the following

process. The aluminum film is anodized in an electrolytic solution to form a fine anodic oxide film 507 having a thickness of about 100 Å on the surface thereof. an ethylene glycol solution containing tartaric acid, boric acid, or nitric acid at 3 to 10 %, in which PH is adjusted to about 7 is used as the electrolytic solution. A thickness of the fine anodic oxide film 507 can be controlled by a voltage applied to the aluminum film. The fine anodic oxide film 507 has a function for improving adhesion of a resist.

After a photoresist mask 508 is formed, the aluminum film is etched by using the mask 508 to form the gate electrode 505 and lower layer wiring 506. In an electrolytic solution, a voltage is applied to only the gate electrode 505 to perform anodization. An acid solution containing citric acid, oxalic acid or chromic acid at 3 to 20 % is used as an electrolytic solution. In this case, since the photoresist mask 508 and the fine anodic oxide film 507 are formed on the surface of the gate electrode 505, a porous anodic oxide 509 is formed on only a side surface of the gate electrode 505. (Fig. 5A)

A growth distance of the porous anodic oxide 509 can be controlled by a current supply time to the gate electrode 505, and thus a length of a low concentration impurity region is determined by the growth distance. The porous anodic oxide 509 is grown at a length of 4000 Å.

Using the photoresist mask 508, the silicon oxide film 504 is etched to form a gate insulating film 510. As shown in Fig. 5B, the photoresist mask 508, the porous anodic oxide 509, and the fine anodic oxide film 507 is removed successively to expose the gate electrode 505 and the lower layer wiring 506.

The photoresist mask 508 is removed using a desired peeling solution. The fine anodic oxide film 507 is etched using buffer hydrofluoric acid. Since the fine anodic oxide film is extremely thin, it can be removed selectively. The

porous anodic oxide 509 is etched using mixture acid that phosphoric acid, acetic acid, and nitric acid are mixed one another. Since the porous anodic oxide 509 can be removed easily, the gate electrode 505 is not etched.

Using the gate electrode 505 and the gate insulating film 510 as masks, an impurity is implanted into the island silicon region 503 by ion doping. In this state, by setting a suitable condition for dose, accelerating speed, and the like, since the gate insulating film 510 serves as a semitransparent mask, low concentration impurity regions 511 are formed just under the gate insulating film 510 and high concentration impurity regions 512 are formed in a region in which is not covered with the gate insulating film. By plasma CVD, a silicon oxide film 513 having a thickness of 2000 to 8000 Å, for example, 5000 Å, is formed as a first interlayer insulator. (Fig. 5B)

Contact holes are formed in the silicon oxide film 513. An aluminum film having a thickness of 4000 Å is deposited by sputtering and then etched to form upper layer wirings 514, 515, and 516. (Fig. 5C)

By plasma CVD, a silicon oxide film 517 having a thickness of 1000 Å and a silicon nitride film 518 having thickness of 5000 Å are deposited successively as a second interlayer insulator. Then, using the first mask, a pattern is formed by a known photoresist method, and the silicon nitride film 518 corresponding to the upper layer in the second interlayer insulator is etched by dry etching to form hole portions 519 and 520. In this state, the silicon oxide film 517 corresponding to the lower layer serves as an etching stopper. (Fig. 5D)

A hole pattern is formed inside the hole portion 519 again by photolithography using a second mask. In the hole portion 520, a hole pattern is not formed. By dry etching, the silicon oxide film 517 in the hole portion 519 is etched to form a contact hole. (Fig. 5E)

An ITO film having a thickness of 1000 Å is formed by sputtering and then etched to form a pixel electrode 521 connecting with the upper layer wiring 515. Thus, in the hole portion 519, the upper layer metal wiring (the drain electrode of a TFT) 515 and the pixel electrode 521 are connected each other. In the hole portion 520, a capacitor 522 (corresponding to a retaining capacitor in a TFT array of an active matrix circuit) is formed between the pixel electrode 521 made of the ITO film and the upper layer wiring 516 wherein the silicon oxide film 517 corresponding to the lower layer in the second interlayer insulator is dielectric.

In a portion 523 that the upper layer wiring 514 (corresponding to a source bus line of an active matrix circuit) intersects on the lower layer wiring 506 (corresponding to a gate bus line of the active matrix circuit), since the silicon oxide film (the first interlayer insulator) 513 having the thickness of 5000 Å serves as dielectric, sufficient insulation can be obtained. (Fig. 5F)

In a TFT of the embodiment, since the low concentration impurity regions 511 are formed between the high concentration impurity region (drain region) 512 and a channel forming region, high voltage application between the channel forming region and the drain region can be prevented, and off current can be reduced.

According to the present invention, contact holes and a capacitor can be formed simultaneously in an interlayer insulator. In particular, a capacitance of a capacitor is increased by the present invention. Also, new added value can be provided with an integrated circuit. The present invention is useful in industry.